sponsored by

Gabe on EDA • EDAmarket

Assembling the Future

A Newsletter About the Design and Production of Electronics

ISSUE 011 • JANUARY 2012

SUBSCRIBE

PDF and Archives

for Printing

twitter

In this issue:

3D Solutions: Or Silicon As Real Estate

Gabe Moretti

In real estate when the price of land reaches a threshold, builders start adding stories to the buildings, even if doing so is more complex and more expensive. I think that the price of silicon has now reached that point, or will very soon.

The Price Of Land

The price of an IC has two components: development cost, and manufacturing cost. Development cost, also called NRE for Non Recurring Expense, is a one time cost that must be amortized throughout the life of the product, at least through sufficient product volume to comply with the price/demand curve that foresees a drop in price once NRE is totally amortized, hopefully before the competition throws a monkey wrench into the gears. Manufacturing costs, though, remain reasonably constant and the only opportunity to lower them is through yield improvements.

Given the semiconductor manufacturing environment the industry has grown accustomed to, the difficulties of 3D architecture would make one quite conservative in predicting a high ramp for this

method. But, semiconductor manufacturing is about to become quite different from the past. The move from 28 nm (or even 22 nm) process to 20 nm and below is proving to be a discontinuity point in our industry. We have reached a limit in the way we can bend light. We are knocking at the front door of X rays (10 nm) without really knowing what we will do when the door is open.

Developing a product for the 20 nm process requires new methods that demand the construction of a team of suppliers that are well integrated and include not just the EDA vendor, more than one make the problem even more complicated, but mask equipment suppliers, test companies, and of course the foundry. In fact the collaboration between the device developing team and the foundry must be so integrated to make any thought of second sourcing unthinkable. We are looking at a different industry, and the impact on electronic companies, EDA vendors, and foundries will be revolutionary. The few remaining IDMs have a less difficult path, but even in their cases it is not a simple path.

So, if one cannot squeeze more transistors on the die, go vertical. As Mike Gianfagna writes in his article in this issue, it may take a couple of years, but 3D is coming. I am more bullish than Mike and think that the market is greater than $20 million in 2014.

Architectural Challenges

To a design engineer accustomed to thinking in 2D, architecting a 3D system will be a challenge. As Admiral Kirk says in The Wrath of Khan, one must be trained to think in 3D, and Khan, to his misfortune, was not. Conceptually the task may not seem as difficult when thinking of the system in functional terms. A typical system will have memory, analog, I/O, and MEMS portions, and digital computational blocks. This could well be the package's three stories.

But things get more complex when one considers interconnects. True 3D architecture uses through silicon vias (TSVs) for die to die connectivity. This means that connecting the top die to the bottom die must take into consideration the geometry of the middle die which must be laid out respecting its own functional and physical requirements. And, of course, connections generate their own problems including EMI noise and power consumption. I would expect that the industry will eventually develop a set of standard connectivity rules, at least as far as memory and computational blocks interconnect is concerned.

The issue then is do we place and route all the dies at the same time, or do we finish each die separately while obeying a set of new rules that reserve real estate on each die for die-to-die interconnect? The latter, at first glance, seems the preferred methods. Certainly it does restrict what can be done on each single die, but the architectural restrictions should not be difficult to live with.

The Test Problem

As the "A New Methodology for Packaged-Device Failure Analysis" article from Magma points out, the problem seems to be testing a stacked die package. The subject was also addressed during last year's GlobalPress conference by Wally Rhines speaking about its company's Tessent product. Wally pointed out that 3D systems need an additional test step before packaging. In addition to wafer test, each individual die must be tested before it is packaged. This additional step diminishes the number of packaged devices that are discarded. In his methodology, package testing will show only interconnect problems since the functional characteristics of each die have been validated

previously. Of course this assumes that system functionality has already been proven before release to manufacturing.

Dr. Rhines stated that all bare die ATPG and BIST tests must be fully reusable within the 3D stack. Since testing of TSV can only be done in-package the system must provide hierarchical ATPG for testing logic-to-logic interconnect as well as BIST for testing memory-to-logic interconnect.

The Role Of Money

As long as it was cheaper to avoid addressing the above problems by just moving to the next process node, companies could choose not to spend money to address 3D issues. Our industry has been described as one that is primarily motivated by technology, not by financial considerations. Cost of innovation has been a necessary characteristic of progress and has been amortized through significantly greater profits justified by increased end product functionality and desirability. Development and manufacturing costs at 20 nm and below are so high that a significant portion of potential products become financially unfeasible. A 3D solution with dies that spans the 90 to 32 nm processes can provide a viable solution and offer consumers a plethora of gadgets at attractive prices.

A New Methodology for Packaged-Device Failure Analysis

Arpan Bhattacherjee, Product Engineer,

and Jim Kramer, Senior Director WW Product Sales Yield Management Business Unit,

Magma Design Automation

As modern day packaged devices become increasingly dense and more complex on printed circuit boards (PCB), multichip modules (MCM), stacked dies, and through silicon via (TSV) devices, the probability of encountering failures on packaged devices is becoming increasingly apparent and challenging.

Failure analysis engineers constantly seek ways to optimize the efficiency of their tools, methodologies, and circuit edits to increase their yield. SystemNav™, Magma Design Automation's new tool for designers and failure analysis (FA) engineers, isolates the sources contributing to a package device's failure or reduced performance. This is partly achieved by enabling the user to rapidly trace signals from a die to a system level and back to die again for fault isolation and repair. After tracing a signal, it enables the engineer to physically navigate the failure analysis tools to specific X, Y locations to determine the root cause of the failure.

Traditionally, a package device consisted of a metal leadframe with dies attached via wire bonds to the metal leads. This technology is well established and the failure mechanisms are well understood. With the advent of devices of more than 100 connections and multiple devices that are combined to a system, there are dramatic changes required to meet current packaging technology requirements. Semiconductor devices are directly mounted on PCBs instead of leadframe packages. Many PCBs are also mounted inside a traditional leadframe package, this technology is also known as *interposition*.

Due to the complexity of these highly dense packages, the manufacturer is typically responsible for the quality and yield of the final package product. This requires a close collaboration between the Quality Assurance and the Failure Analysis teams to analyze the multiple devices on the packaged product.

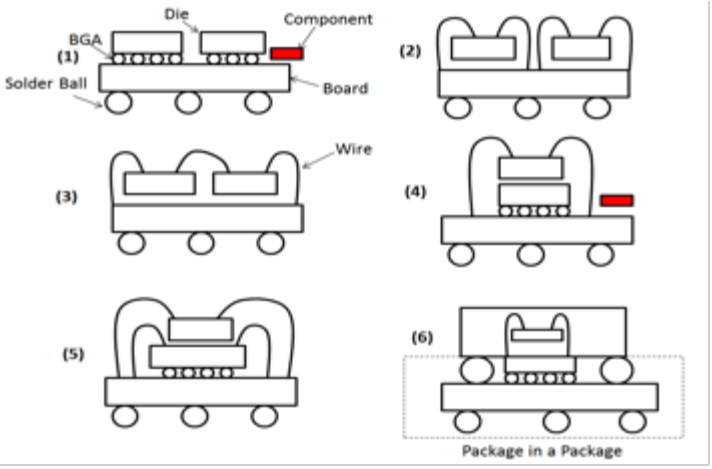
Package devices are reaching dimensions that typically require IC Failure Analysis methodologies and tools. In addition to multiple stacked die and TSV devices, embedded passive components within multiple PCB layers add a new level of QA/FA complexities and challenges. More than 1,000 connections are becoming a standard for modern packages. All of the technological changes mentioned above lead to challenges in the FA process.

Similar to Magma's Camelot™ IC-based CAD navigation tool, SystemNav utilizes its core IC failure analysis and circuit edit capabilities on packaged devices, allowing seamless navigation and CAD-supported fault localization at a system level with chips and PC boards. Electrical signals can be traced from the board to the chip as well as between chips; following all types of connection methods, such as flip chip mounts, wire bonds and TSVs. Images of inline defects and thermal images can be overlaid to the layout data. With additional features such as 3D cross-sectioning analysis and schematic cross mapping, the tool is able to visualize multiple layers of a small area. It can overlay inline images to electrical traces, cross map schematic to layout to isolate and study fault mechanisms, and communicate to FA tools for accurate CAD navigation.

FA teams working within semiconductor companies are responsible for the final package that consists of one or more silicon chips mounted on a PCB. CAD supported navigation on analytical equipment is the "de facto" standard for CAD data viewing and CAD based analysis. With SystemNav, the technology of CAD navigation is now expanded to not only analyze the chip but also the PCB on which the chip is mounted.

Quentin Saulnier at STMicroelectronics notes: "With more and more functionalities and less and less space, we are always facing new challenges due to the introduction of multichip modules and systems in package. Some of these new challenges are due to the interconnections between the die inside the package and others are to the specificities linked to stacked die. Nevertheless, we have to go more and more into the comprehension of the package and Magma's SystemNav is a tool that is allowing it. That's why we've started to evaluate SystemNav with promising results."

A multichip module/PCB can be designed in the following configurations:
(1) Multiple die on board (BGA)
(2) Multiple die on board (wire bond)
(3) Die to die connection
(4, 5) Stacked die (wire bond/BGA)
(6) Package in a package

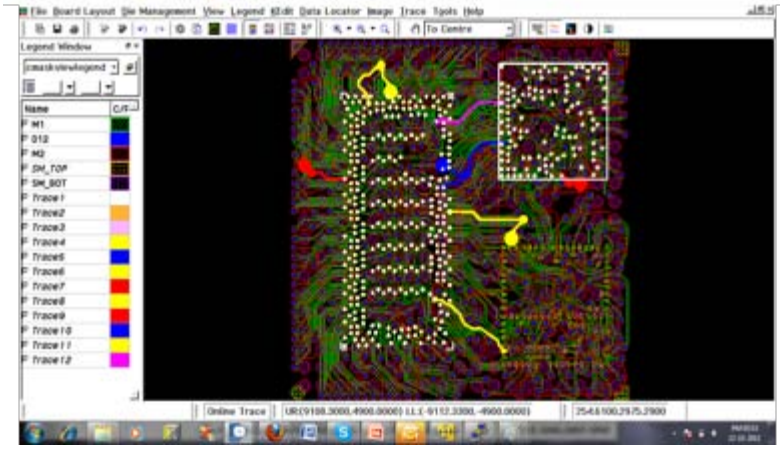


[Figure 1]

The following graphic depicts a parallel section of an inner PCB layer and shows a crack has propagated through these copper traces. With SystemNav, the layer can be isolated, aligned and overlaid on this image. The tool then communicates with the customer equipment interface (i.e. Focus Ion Beam) to make the necessary circuit edits to repair the fault.

[Figure 2]

Parallel section of an inner PCB layer showing crack.
Source: Sem Lab, Inc. (http://www.semlab.com/example22.html)



[Figure 3]

CAD View of PC Board

The image above shows the graphical user interface of a PCB layout. The white nodes represent the PAD layer connections of the die that is placed on the board. The red, yellow, pink and blue signals are highlighted traces of the selected nets of study. Note that the pink and blue traces highlight connections between two dies, both of which are placed on the same board.

As this article highlights, failures on packaged devices is becoming increasingly more prevalent and failure analysis engineers are looking at a means to optimize the efficiency of their tools to increase yield. Magma's SystemNav isolates sources contributing to a packaged device's failure or reduced performance.

3D: The Cart Before the Horse?

Mike Gianfagna

Vice President of Marketing Atrenta Inc.

San Jose, California

Stacked die 3D design is hot. Everyone is talking about it. There are panels, blogs, conferences and articles galore. 3D technology holds the promise of avoiding the train wreck that will occur when Moore's Law runs out of steam. The technology is fascinating, the design problems are substantial and the possible products are mind-bending. From an EDA perspective, there is a lot going on. Lots of companies (including Atrenta) are spending time and resources to come up with new, advanced tools to address the unique challenges of 3D.

But when will all this work pay off? When will 3D design move into the mainstream? As a supplier of design tools, this is a very relevant question. One that my CFO asks me all the time. So I did a little investigation, estimation and analysis. Throw in a little educated guesswork and you have the complete picture. Here is what I found…

Today, there are precious few 3D designs in production. For those that are available, bare die on silicon interposer is the technology of choice. This is not quite 3D; more like 2.5D. So when will true stacked die, heterogeneous 3D chips hit the mass market in high numbers? Well, nobody really knows. The best we can do is triangulate the trend from secondary principles. Here's where the educated guesswork comes in.

Let's start by looking at the ITRS roadmap. The ITRS (International Technology Roadmap for Semiconductors) 2009 edition predicts that 3D design space exploration moves from development to continuous improvement in 2013. Furthermore, ITRS, as well as many other sources, predict that 3D

sees traction at 45nm and below. So, let's see what that could mean from a market opportunity point of view. By 2014, there will be something like 800 design starts below 45nm. Let's assume (conservatively) that 5% of those starts have a 3D component and further assume a $500K design tool seat cost for those advanced designs. This yields a market opportunity of $20M. It's starting to get interesting, but you have to wait two years.

So, if you have the patience to wait a couple of years, where will the action be? Thanks to a study GSA did, it appears that cell phones will be a big consumer of these kinds of devices. Not that surprising I suppose. Will 3D be worth the wait? I believe it will. Single chip, monolithic design will become much harder as we approach the end of the road for Moore's Law. Divide and conquer strategies like 3D will be the answer to a lot of tough questions.