sponsored by

Gabe on EDA • EDAmarket

Assembling the Future

A Newsletter About the Design and Production of Electronics

ISSUE 016 • JUNE 2012

SUBSCRIBE

PDF and Archives

twitter

In this issue:

DAC 2012 A Retrospective

Gabe Moretti

Having attended well over thirty DAC conferences I have come to let a few weeks go by before I attempt to distill the essential messages from the event. The bottom line is likely to surprise many. Financial considerations are now as important as technical consideration when planning a project targeting the 20 nm process. Electronics has always been an analog technology that could stand digital approximation at larger transistor sizes. Mainframes and minicomputers of the sixties and

seventies are now IC platforms using multiple cores and a significant portion of IP, which makes software development the real bottleneck in product development.

Costs and Capabilities

At last year's DAC people were talking about how the higher difficulties of designing for 20 nm processes would be compensated by improved execution speed and significantly greater functionality. At this year's DAC foundries and EDA tools vendors spoke of the much higher collaboration required among them in order to provide a production worthy flow to the industry. No one could show a product at 20 nm, and foundries were more reserved and conservative than EDA vendors about volume production at this node. There was also practically no more mention of 14 nm work targeting third party designs. Reality is beginning to settle in the industry. The appeal of moving from one production node to the next was based not only on technical advantages, but economic factors as well. Every new production node yielded a lesser cost per transistor for the product. But early results at 20nm show that a transistor at this node may cost at least as much as one at 32 nm, and may be a bit more.

As economic considerations enter the decision process, EDA vendors will face a different market. One not only guided by the need to follow technological progress, but one that must consider the probability of profit and the size of it when deciding if and how to develop a product. As foundry dependency increases due to the personalization of the fabrication methods, well integrated teams will develop. They will include the product company, the foundry, and the principal EDA vendor. Startups will find it more and more difficult to compete in the RTL to GDSII market segments. Only clear superior technology can result in success, where success will be through an acquisition by one of the three leading vendors.

Platforms and IP

Production volume is one of the fundamental parameters in the financial equation determining whether a product will be profitable or not. The ability to distribute development and pre-production costs among a large quantity of die is key in determining the break even point and subsequently the size of profits possible. But in a fickle consumer market where a product has an expected life time of less than eighteen months reaching break even at a competitive price point may require over a million units sold.

As we are seeing starting at 65 nm and certainly at 45 nm process nodes, IC's are becoming less application specific and contain more general purpose hardware that is then tailored to the application by software. With very few exceptions this will become the common architecture at 20 nm and likely beyond. This means that both system level tools as well as emulation and verification tools will represent the larger expanding market in EDA. The verification bottleneck has yet to be solved efficiently, and in fact continues to increase in complexity. Atrenta, as an example, has recognized this market reality and has re-branded its Spyglass product transforming it into an extendable verification platform.

This trend favors the growth of FPGA based products as well as third party IP companies. Both Altera and Xilinx are offering very sophisticated development tools. Xilinx during GlobalPress 2012 announced the Vivado design suite which not only provides a complete methodology for FPGA based design development but also allows companies like Blue Pearl Software to find an expanded

market for its products.

Three Dimensional World

An IC has always been three dimensional, even the flat world society admits that nature is not two dimensional. At the 2011 GlobalPress Conference I heard a good presentation by Wally Rhines of Mentor about 2.5D methods for IC packaging. Since then I have read and listened to a number of presentations about 3D ICs. At DAC Cadence described to me its latest strategy to support 3D IC's.

My first impression is that 2.5D methods may be a way to extend the life of the 45 nm process well beyond its traditional expectancy. Packaging one die on top of another and using an interposer to provide the connectivity sounds like a technique that is not tremendously difficult to implement. Such method could allow, for example, to package a large portion of memory with a SoC platform, or could allow the use of two separate processes to integrate analog and digital functions.

Taking a clue from the PCB world, where boards with 12 interconnected layers are no longer "state of the art", IC architects could even extend the technique to packaging a three layer IC.

But I think true 3D devices, using through silicon vias are still a few years away. The reason is that IC architect have not learned to think in three dimensions, and thus the optimal partitioning of a design among various layers of silicon cannot be commonly achieved to the point that a new design and manufacturing method can be economically sustained. Technically the Cadence presentation was sound and credible as a long term road map, but much remains to be done in educating designers to think in three dimensions.

Everything is Analog

As second and even third order effects have become required areas of concern in digital design, engineers are discovering that simply knowing how to program in Verilog or VHDL is no longer sufficient to produce a working IC. Both large and small companies at this year's DAC exhibited analysis tools dealing with issues such as power consumption, clock distribution, analog simulation, and all other DFM, and DFY physical characteristics. I found of particular interest the approach taken by Uniquify, a company that is like a fabless foundry. Their approach could be described as DFP or Design For Profit. They provide development services to system houses that are targeted to achieving technological and economical success in the shortest possible time.

In the analog simulation domain I was positively impressed by Infinisim and Orora. Infinisim is a very small company that offers a very fast SPICE equivalent simulator, while Orora, based in Washington state, is building a credible track record in analog behavioral modeling, analog design analysis, and SPICE equivalent simulation.

Sino-American Company

ICScape was a new exhibitor this year and it attracted a lot of attention, but not just for its products. The company offers tools for design closure, specifically for timing analysis and clock insertion. The company, started in the US in 2005, merged in January of 2011 with Huada Empyrean Software, a Chinese company. Huada is a subsidiary of CEC the largest electronic conglomerate in China with over $23 billion of revenue in 2011. Huada itself has $28 million cash on hand to invest in growing

the company and its markets both in China and overseas.

ICScape thus is now a well funded startup, it is like getting a second round for free! What needs to be seen is how compatible the demands of the Chinese market are with those of the US market. Will Huada and ICScape have a happy and productive marriage, or will it end in divorce? It almost does not matter, since their approach is likely to be followed by other companies as the Chinese market for EDA continues to grow and as the availability of trained engineers and investment capital in China seem to be plentiful.

Standards

Si2 celebrated the tenth anniversary of OpenAccess. Originally donated by Cadence the data base has been responsible for a large number of startups who saw, and see, a direct opportunity to be compatible with an entire design flow through the OpenAccess interface. Although some do not consider Si2 a proper standard organization due to its restrictive distribution policies, it must be recognized for having contributed significantly to the growth of the EDA industry. Si2 held different seminars during Monday covering its areas of activity. In addition to the OpenAccess project, the consortium is active in areas including design for manufacturability, low power, 3D design, and Open PDK. This last one may be facing an uncertain future at 20 nm and beyond, since process details may vary from foundry to foundry to such an extent to make designs non-transferrable.

During the conference Accellera announced the release of the Unified Coverage Interoperability Standard (UCIS) 1.0. It is the first standard released since the merger with OSCI and shows that the consortium has not lost its focus on supporting the EDA industry with open standards destined to become IEEE standards. During its luncheon event on Wednesday Accellera presented its first Accellera System Initiative Leadership Award to Dennis Brophy, a founder of the consortium. Dennis has been a leader in the area of EDA standards for over twenty years and is also a board member of the IEEE Standards Association and Chairs the Corporate Advisory Board of the organization.

Attendance and other less important things

The DAC Executive Committee pays great attention to the attendance numbers, as if this is the best way to measure the conference success. The preliminary numbers show that conference attendees were 1901, up 9% from San Diego, while exhibitors' booth staff was 2704 up 11%. I suppose that conference attendees come to hear the papers and follow the technical sessions, so the impact of these two categories on each other is only a secondary effect. What is interesting is that a location close to Silicon Valley combined with the efforts by Atrenta, Cadence, and Springsoft to provide free access to the exhibits has had a significant impact on exhibit attendance which was up 39% over San Diego to 2783. Increased exhibit attendance requires increased exhibitors' staff. Increased staffing was also made possible by the fact that the staff was mostly local, thus decreasing significantly the travel expenses of the exhibitors.

The FortyNiners Goldrush Cheerleaders Squad unwittingly provided the most significant controversy of the conference. Their performance at the beginning of the plenary session was announced and then cancelled after an informal protest about sexual stereotyping launched by Peggy Aycinena. The performance was an example of how DAC Executive Committee is trying to raise attendance. Transforming DAC into a consumer oriented marketing show counting on a testosterone rush to increase attendance has now been officially shown to be a failed idea. Had the Executive

Committee dedicated about fifteen minutes to think about this idea, they would have avoided the fiasco.

In my opinion it is time for Cadence to retire the Denali Party. Another example of libido that has outlived its time, the party had significance when a small and very successful company like Denali created an environment of relaxed camaraderie among attendees. Cadence's corporate profile just does not fit the party atmosphere. The company has arrived to its destiny as a reliable provider of EDA tools jousting with Mentor to be number two in the industry. The future will not be significantly different a year or five years from now: the future is now. Sanjay would have seized the opportunity and had the GoldRush at the party! This is the difference between Denali then and Cadence now. Cadence personality is not reflected in the Tuesday evening party. Why not instead be the official sponsor of the DAC party on Wednesday?

San Francisco Great Locale for DAC

Lauro Rizzatti, General Manager of EVE-USA

This DAC may have been the best ever for EVE, noted for our ZeBu hardware-assisted verification platform. San Francisco is always a great locale and everyone seems to arrive in good humor.

The EVE booth team collected more leads than we did last year and many of them we consider to be hot leads. We captured the attention of attendees who just happened to be verification engineers from around the globe over those three days and scheduled numerous meetings with them to see how we can meet their challenges. Attendees claim to have budgets, something we haven't heard lately at DAC.

Other verification companies are in the partnering mood. Several approached us during DAC about cooperatively building accelerated verification solutions across a broad spectrum of challenges. One attendee was impressed with our partnership with the EDA industry's leading vendor.

We had a perfect booth spot, despite reservations about being directly across from one of the big three's theater. After each presentation, the crowd would turn around and look to see what we were demonstrating. As a result, our presentations each day were packed.

The industry has been hearing for years that verification is the bottleneck in a design project schedule. For the first time, perhaps, engineers came to DAC to check out verification tools and strategies instead of design tools. They also need tools that can be used by the entire team that today include both hardware engineers and software developers. EVE is well positioned for this seismic shift because these engineers are finding that emulation is the only verification tool to offer hardware/software co-emulation.

Additionally, many were talking emulation and prototyping, key market segments for EDA, and we

have a solution that straddles both. One more obvious trend is toward power-aware verification or ways to check functional integrity of multi-power domains, something EVE's ZeBu can handle.

Many attendees were interested in learning more about our vertical solutions, including transactors and ESL integration, which leads us to conclude that verification tools need to be part of an environment, something we haven't heard before.

One element missing from this year's DAC stew was a stunning pre-show acquisition that previously sent quivers through the industry. DAC was a success without it. Afterward, the industry was treated to the news of the acquisition of one verification vendor by another.

One EVE executive summed up our experience at DAC this way: DAC 2012 was a good vintage, good number of visitors, quality attendees and good organization with hotels close to the Moscone Center. He added that our public relations efforts fit attendee expectations about market trends.

We look forward to Austin for next year's DAC. The challenges affecting verification engineers will hardly be solved in a year. EVE will work hard to continue to provide solutions aligned with the needs of attendees.

DAC 2012: Finally enabling the customer

Mike Gianfagna, Vice President of Corporate Marketing, Atrenta Inc.

Momentous, enlightening, possibly game-changing. One could characterize DAC 2012 this way. And not because of cool new point tools, but rather because of the collaboration that was felt on the show floor.

First and foremost, it was heartening to see much greater focus on ***all*** aspects of completing and delivering a design and not just on the design tools. That the industry may finally be focusing on what it takes for a customer to construct a process or methodology focused on the whole job of generating a design from concept to package delivered silicon is encouraging.

This DAC was also notable because other key members of the design ecosystem participated. Discussions centered on how design and manufacturing need to work closely to provide customers with the tools and services to get 2012-and-beyond SoC designs out the door, manufactured and into end-products.

Foundries, along with design services, FPGA and IP providers participated. TSMC, with its theater-style forum, highlighted the vast number of partners it works with for the customer's benefit. Global Foundries was there, too. And there were a number of small silicon service companies and small ASIC companies – vendors who are going to take your RTL design to a foundry. We saw major vendors like ARM, Xilinx and Altera whose presence showed that they care about how customer-

oriented design enablement has to emanate from cohesive cooperation among the different vendor types.

What's driving this all? Complexity is, pure and simple. That is why we are seeing IP vendors and some of the bus fabric providers join the discussion. I think the complexity of managing deep submicron is why we're seeing TSMC and Global Foundries at DAC. The cost alternatives are why we are seeing Xilinx and Altera show up. You can't decouple the SoC problem into the design tooling piece vs. the manufacturing piece vs. the rest of the supply chain.

Power was acknowledged as a huge problem and will continue to be going forward. We are nowhere close to saying that the power problem is solved. We had huge attendance in our SpyGlass Power suites, but not only from the mobile end-product vendors. We are starting to see server and base station applications becoming much more power sensitive. To varying degrees they're not at all trying to do what the mobile vendors are doing. But they are all now having to concentrate much more on power management and optimization.

For these designers, cost rather than extended battery life is the prime objective. A data center, for example, could save millions of dollars over its life by reducing server power. In the case of base stations, you are talking about units that are literally sitting up on mountain tops or somewhere in the wild. Powering these facilities costs money, but in a very different way than the cost of battery life.

What was clear at DAC 2012 is that RTL power optimization is important. Several years ago, it was a nice-to-have. Today, it's a must-have. And we see customers wanting an entire integrated suite – or platform – of RTL tools to handle the power issue, namely: power verification, estimation and reduction. So customers looking to solve their upcoming power problems – and that's virtually everyone – now have an essential two-item checklist: 1) find vendors who work closely together as part of a vibrant ecosystem; 2) find a tightly-integrated platform of RTL tools.

DAC Offers Visibility and Priceless Opportunities

Bob Smith, Vice President of Marketing, Uniquify Inc.

Although Uniquify is not an EDA vendor, we look forward each year to exhibiting at DAC because we find it's a great place to build visibility and awareness.

This year was no exception. We were in the corner booth on a well-traveled aisle that included our friends at Verific. While we had a chance to mingle with many DAC attendees, we enjoyed watching the Verific team try to explain why the stuffed animal giveaway didn't look much like the Verific mascot, the giraffe!

Since its founding in 2004, Uniquify has hired a talented and motivated team, many of whom helped out with our presence at DAC. Not only did we have our own booth to staff this year, but a presence

in three additional partner booths. It was a long three days, but productive, stimulating and fun. Uniquify's known for working hard, getting great results and playing hard when the day's over.

Fun is a watchword at Uniquify, something we don't often equate with EDA or the semiconductor industry. To prove that we like to have fun after a long day, we hosted the first Uniquify Party at DAC at the Lava Lounge and it was a great success.
The idea for a party came from Denali, our role model that's now part of Cadence. The similarities between Uniquify and Denali are striking. Similar to Denali, we have a team of about 90 mostly technical employees, many of whom have worked together for years. And, like Denali, we work hard, but we also like to have a good time.

As a marketing executive, I appreciate the value of giveaways and drawings at trade shows such as DAC. Without them this year, the crowds at various booths would not have materialized, I'm sorry to report. I saw the same scene repeat itself in different booths at different times: The presenter starts talking; people gather; the presentation ends and either a gift is handed out or there is a drawing; and then everyone leaves.

This leaves me wondering about the quality of the leads or the marketing strategy.
Perhaps the most novel approach to gathering interest was put on by Oski Technology that took an RTL design from NVIDIA at the start of DAC with the challenge to complete verification in 72 hours. The designer and workstation were live on webcam throughout DAC. A skeptical engineer actually called the designer via mobile phone only to watch as he answered live on the webcam.

As a result, the Oski booth appeared quite busy throughout all of DAC. Let me mimic a MasterCard commercial: At a conference full of memorable sights and sounds, Oski's promotional effort was priceless.

Denali used DAC as the place to host its yearly party and built its brand around it. With so many other similarities, you can expect to see Uniquify continue party at DAC. Meanwhile, keep close watch on Uniquify because you're about to hear more from us, and it won't be only about next year's party. Next year, our promotional effort may be priceless.

Breaking Systems at DAC

Adnan Hamid, Chief Executive Officer, Breker Verification Systems

We went to DAC this year to break systems. No, not the DAC system, but systems as in systems on chips (SoCS), and we succeeded! Over three days, we gave numerous demos, met with a large number of verification teams and began to forge partnerships with other key EDA players. Anyone who saw us at DAC previously may not recognize us any longer. We are now The SoC Verification Company. Our goal is to remove functional verification as the bottleneck for technological innovation and project schedules, especially those challenges associated with complex SoC designs. That

means breaking systems.

The difference this year is momentum. We closed calendar year 2011 with year-over-year growth of more than 150%. In previous years, we hailed from Austin, Texas, where DAC will be next year. Late last year, we relocated to Silicon Valley to be where the action is. And, what action! We're now closer to a strong customer base and unique opportunities. We stepped up the pace, increased our visibility and continued breaking systems. Just in a different location.

Our booth was located on a main aisle, but in a relatively quiet corner. Recognizing our unique products, Gary Smith EDA included us in the "What to See at DAC List," which helped drive attendees to our booth, some with the printed list in their hands. Gary also recommended Breker at his Monday morning presentation, and John Cooley added us to "My Cheesy Must See List for DAC 2012." Those who did stop by to see us were serious about their verification challenges. And, everyone who came by the booth wanted to see us break systems.

Many attendees asked us how we came up with the name Breker Verification Systems. My nickname in graduate school was Breaker — yes, for breaking systems — and that morphed over time into Breker. We used that history to our advantage at DAC by greeting everyone who stopped by the booth with, "Have you heard of Breker? We break systems!"

Sure, we noticed that the DAC exhibition space was smaller and there were thinner crowds than previous years. However, we were happy with the contacts we made. Gary and John get some of the credit for mentioning us, but I also believe that the industry is catching up to the solutions that we offer. From what we saw at DAC, the EDA industry continues to focus on block-level verification, even with the rapid growth of SoCs with multiple embedded processors.

When multiple processors and many different types of IP are involved, methodologies in use for block-level verification break down. That's precisely where we step in to break systems and find tricky system-level bugs before tapeout. More and more companies are hitting the verification wall and looking to Breker for help. I fully expect this trend to continue.

You can bet that we'll be in Austin next year, ready to break systems once again.

Bagpipers a DAC Tradition

Brett Cline, Vice President of Marketing and Sales, Forte Design Systems

I can almost hear the last strains of the bagpipes as DAC came to a close this year.

Rich Davenport, a friend, long-time EDA executive and former CEO of Simulation Technologies and Summit Design, officially introduced me to the closing of DAC with bagpipes in the late 1990s. We

used to go to the HP booth at the end of the show and listen to it blast over the sound system and it was great. The tradition continued when I joined CynApps and attended DAC in 2000. A bunch of friends would meet there and enjoy the fun until one year it didn't happen.

Forte's been sponsoring a live version of the bagpipers' performance since then. Moreover, we used the same bagpipers every year from 2003-2011. This year, they couldn't make it due to a scheduling conflict, so we found a local grandfather and grandson to fill in and they were great as well. Now, just about everyone left on the floor comes over to see the closing of the show. It really is a DAC tradition and we love doing it.

Bagpipers are a tradition in New England, where I'm from, and often march in our local parades for a bit of old mixed with new. Despite what you may think, bagpipers aren't a bunch of old codgers looking for an excuse to get out of the house. This year's DAC bagpipers were a team that married old with new.

Bagpipes, then, serve as a perfect metaphor for DAC — traditional, tried and true technology mixed with new and emerging technology or a link between technologies.
Traditional technology? Simulation, logic synthesis and design rule checking that date back to when exhibits were first introduced at DAC in the mid 1980s. The new technology includes SystemC and high-level synthesis. I'd add virtual prototyping as well. Some readers may say that ESL tools such as these have been around since Gary Smith coined the term in the late 1990s.

While the term has been around for quite a while and we certainly hear plenty on the topic, it's only recently that commercial HLS software has become widely deployed. And, it's now going main stream. Design teams worldwide have adopted the technology for large, critical portions of their designs. That's because today's HLS provides results that are better than hand-coded RTL and includes control and datapath support, hierarchy support, custom TLM interfaces and other advanced features too numerous to list.

Forte's booth traffic this year was a good example of the interest in HLS by DAC attendees. We had a constant stream of attendees who wanted to see demos highlighting the benefits of SystemC-based high-level synthesis. Our demo was based on a real-world example that used an ARM-based image processing system with multiple control- and datapath-type blocks connected with line buffers, and other sophisticated interfaces. In addition, we hosted a session where a hardware designer offered a look at how he used high-level synthesis for the design of a USB 3.0 controller. Other exhibitors stopped by as well to see what kinds of partnerships could be forged.

Our DAC giveaway is as memorable as the bagpipers. Each year, we hire a caricature artist that is always a great hit. We did well over 100 caricatures in two days this year. This tradition started as we were looking for something memorable. At the time, caricatures weren't being done much at tradeshows. And, now they have evolved as much as HLS has. The first year, it was traditional with paper and a drawing pencil. Since then, our artist not only has a team of other artists that he works with but, in true DAC fashion, has gone digital. We've seen various tablets and an iPad used. This year was a combination of a high-end drawing tablet and an 11" Macbook Air. Not only do attendees get a printout of their caricature on the spot, but they can also download the digital version from our website. Very cool.

San Francisco is always a great place for DAC, and this year was no exception. We saw high-quality

attendees and we were very busy. Booth traffic was great for most of the show, but there were dips near the end of the week and during keynotes. Our suites were at nearly 100% capacity the entire time.

The DAC Executive Committee did a great job getting the word out and making it easy to get people from Silicon Valley to San Francisco.

I believe that this is the third straight year that attendance numbers were up, so it is not just a San Francisco phenomenon. I'm looking forward to the 50th DAC in Austin next year. It's a new location and there's a large engineering community that may not usually travel to DAC. The planning is well under way and most of the vendors that I spoke with are excited to head to Austin. You can count on Forte to provide the poignant end to DAC in Austin once again. Stop by our booth at the end of DAC and be part of the tradition.

DAC Offered Opportunity to Show Oasys Right Here, Right Now!

Paul van Besouw, President and CEO, Oasys Design Systems

The Oasys team stepped out of the Tiki Hut from last year's DAC and into a sleek, industrial-looking booth to show that we're "Right Here, Right Now!"

Exhibiting at DAC is annual ritual of the EDA community and enables companies such as Oasys to show that their tools are real. That's why "Right Here, Right Now" took on great importance for us this year. Every designer's dream is to synthesize RTL directly without the need to partition it into bite-sized blocks, and in hours not days. That's what Oasys with its 100-million gate capacity enables designers to do and that's what we were demonstrating over the three days of DAC.

Our first-ever floor demos showing why Chip Synthesis is a fundamental shift in how synthesis is applied to the design and implementation of ICs were well attended all three days and the feedback positive. The demo highlights the benefits of RealTime Designer, the first design tool for physical RTL synthesis of 100-million gate designs. It produces better results in a fraction of the time needed by traditional logic synthesis products through a unique RTL placement approach that eliminates unending design closure iterations between synthesis and layout.

While we were kept busy, overall attendance this year was okay but not terrific, or so we thought. Booth traffic was high Monday because of San Francisco's proximity to Silicon Valley. According to our sales team, the seniority level of the attendees was not much different than last year, a bit disappointing given the locale.

Another annual ritual is the exhibitor scramble to make the EDA industry influencers lists. This year, Gary Smith and John Cooley both gave us thumbs up, reinforcing our "Right Here, Right Now"

theme. We made Gary Smith EDA's "What to See at DAC List," as well as John Cooley's Cheesy Must See at DAC list.

You may have stopped into our Tiki Hut last year at DAC for a smoothie, a big hit that often sold out before the show closed for the day. We opted to give away key-ring flashlights that were an equally big hit and ensured all DAC attendees could see that we're "Right Here, Right Now."