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Assembling the Future

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Times Are Changing

Gabe Moretti

Pope Benedict XVI has shown great courage in deciding to retire while he can still do useful work in another function. I am going to follow his steps. Therefore this will be the last issue of "Assembling the Future" and as of February 28 also the end of the EDAMarket service from GABEonEDA.

I have reached this decision following a number of considerations, but two of them stand at the forefront. As many of you know I am an avid cruiser. To see a growing number of people with limited mobility on a cruise ship has made me conclude that I want to cruise while I can fully participate in the activities, and no longer.

If for my wife Linda moving near Sarasota was the opportunity to influence a great, if small, American Opera Company, for me it meant a four hours drive to Port Everglades. For example this year I will be gone from April 28 to June 12, both cruising and visiting parts of Italy I have not yet seen. It would be very unfair to my customers to leave them before and during DAC without the services they have paid for.

Secondly, the communication business in EDA is in a state of flux and is not showing any sign to settle. This is mostly due to the unwillingness of the constituents of the industry to admit the

obvious. The industry in very few short years will be unrecognizable from the one that existed just fifteen years ago.

But I have not spent 45 years in EDA just to totally walk away from it. I will be around and plan to offer my help when needed, but not in a full time capacity. So, if you have any ideas, let me know.

I started developing EDA tools in 1968 and have seen the industry come into existence, grow out of proprietary workstations and become a business centered in developing software tools. Most of the tools came out of startups that made a lot of money for the entrepreneurs: engineers, marketing, and financial people with the courage to follow their visions. Then sales and financial capabilities took over, and the three best positioned companies came to dominate the industry.

The time of large multiple rewards for EDA startups is over. Cadence, Mentor, and Synopsys can now either directly compete or profitably co-exists with tools from smaller established vendors. This will be much more obvious at 20 and at 14 nm processes. The long and deep cooperation between product developers, semiconductor manufacturers, and EDA vendors required to produce a financially successful product will further restrict the potential for small and certainly startup companies. The amount of money needed to become and remain competitive will continue to increase.

This has generated a new requirement in the way companies communicate to the market. Marketing money is concentrated in few companies whose primary objective is to maintain their installed base and to influence the financial markets. Thus proprietary corporate events are more frequent and will become more important while conferences like DAC and DesignCon, for example, will loose much of their marketing appeal and become pure technical events.

How they will solve their own financial problems is an interesting topic, but it is clear that the present model has given loud warnings of fatigue and diminishing returns on investment.

Of course you can expect that I have my own ideas about what the EDA industry will look like five years from now. After all I cannot become someone else and just walk away. I believe that taking a step back and calming the emotions, spending more time studying economics and philosophy and writing, will produce great results, even when dealing with EDA. And of course these are things I can do on the decks of a cruise ship!

Verified Beyond Doubt

Dr. Raik Brinkmann, President and Chief Executive Officer,

OneSpin Solutions

What design team doesn't have the desire – make that goal – to have a chip that works as intended and taped out in just one spin? Come on. Let's be honest: They all do!

Well then, let's focus on the methodology and tools to meet that goal. I contend that this lofty goal is met only through a solid verification strategy, with specific goals and with the tools that support the strategy and goals. After all, verification takes a vast amount of time to fully prove the chip design works as the specification stipulated, and shouldn't be dismissed as a "must do" tactic instead of a "must have" strategy. Instead, it must be seen as a way to ensure the correctness of a design, to reduce cost by eliminating respins or mask sets and to improve time to market.

Semiconductor companies have come to rely on savvy verification experts who know that formal verification and assertion-based verification are key components to a successful tapeout. Better yet, the EDA community is responding with production-worthy formal verification software, ensuring designs are verified beyond doubt.

Assertion-based verification is experiencing widespread acceptance after going through an initial industry hazing, much like every other formal verification software had to do. It was seen as too difficult to use and too specialized to be effective. The more experienced chip designers and verification engineers stuck with the tools they've always used. It came down to the more junior team members to give it a try.

The tools have evolved since then from an "expert-only status" where experienced application engineer from the supplier needed to be on site to run them to becoming more usable for the entire design and verification team. Teams evolved as well as they started to see the merits of assertion-based verification and began using it earlier in the process. They had to because their SoC designs contain more silicon IP blocks. While blocks of silicon IP have become great productivity enhancers, presumably reducing project schedules and budgets, design teams need to be concerned about the quality of the original verification of that piece of IP.

Many formal tools are applied as push-button solutions for various tasks and not limited to IP block verification but extending to full-chip integration, such as connectivity verification and X-verification. Yet, IP blocks are pre-verified and, as such, bring many advantages because the verification of that block is not a task for the integrator. Therefore, the focus on high-quality IP blocks is a priority for SoC designers and verification engineers. That's the reason why they rely on push-button solutions targeted toward IP creators who are either part of the SoC design house or their suppliers.

However, more and more verification teams see this challenge. And, as they become more comfortable with these tools, they've started to move to a deep formal approach, or the ability of formal verification tools to take on a higher level of technology to verify the complexity of functions. Deep formal offers verification teams a scalable and flexible formal environment that ranges over all aspects of formal applications, from push button solutions to deep formal and transaction verification.

As a result, verification software and assertion-based verification have become part of almost every verification team's arsenal of tools. If they are not, they have been budgeted and are on the evaluation schedule.

Even so, EDA is falling behind in the verification space and could do more. All forms of formal

verification are needed, from logic equivalence checking to assertion-based verification, a tremendous opportunity for the entrepreneurial inclined. Few formal verification tool providers currently offer a deep formal approach.

The verification community will soon gather once again for DVCon in San Jose, Calif. Attendees can expect to see a variety of verification suppliers with some new, some older tools to support their needs. One will be OneSpin Solutions, a company committed to verifying the chip works as intended and is ready for tapeout in just one spin. Hence, the name OneSpin Solutions. Stop by the OneSpin DVCon Booth #405 to better understand how OneSpin Solutions can help you meet your verification goals.

Formal Verification and Validation

Gabe Moretti

I got my first demo of a Formal Verification tool in the spring of 1992. It was given by Paul Menchini of VHDL and other IEEE standards fame. No one could accuse Paul of not understanding the theory or not being familiar with CAE tools. Yet, the demo showed how difficult it would have been to use the product. This was not something peculiar to the particular tool. The early formal verification programs were difficult to use and had almost nothing to do with hardware design. Even a highly respected "language lawyer" like Paul found navigating within the formal rules challenging.

So in the 1990's it seemed like formal techniques would remain esoteric and limited to people with very good understanding of mathematics and modeling languages. But need is a powerful imperative and EDA developers are highly creative. The first decade of this century has seen a significant growth in both formal technology and formal products. Formal became a separate market segment and a number of startups lead the way. Both verification and validation of hardware design became accepted and used by a large section of hardware developers. The article by Dr. Raik Brinkmann in this issue describes the hurdle formal verification had to overcome, the acceptance it acquired, and the role it plays today.

Yet, today one does not hear much about formal verification as a separate technology. It has matured and found its own position within the Verification market. There are still a few companies that specialize in formal technology, but with the passing of time they are becoming identified within the verification market. Formal tools are no longer talked about separately, as requiring additional expertise. They are part of both development and verification methods, they are accepted just as logic simulation is accepted. The products are user friendly, follow hardware development methodology, and are well integrated in the design and verification flows.

The maturity of the technology is best exemplified by the IEEE 1850 standard that offers a validation language called Property Specification Language (PSL) used to describe verifiable characteristics of a design and it is usable with all popular hardware description languages.

The upcoming DVCon, sponsored by Accellera, is a good place to talk about formal techniques with peers and vendors and see the advances in the technology and the seamless ways it can be integrated in the design and verification flow.

The Market

I seem to remember that according to Gary Smith the formal verification and validation market was worth about $150 million last year. This again is an example of how some products incorporating formal techniques are now classified under a different market segment. In addition to Cadence, Mentor, and Synopsys, my search of EDA vendors that offer tools or overtly use formal techniques yielded eleven companies. Two of these, namely Atrenta and Jasper Design Automation, have sales in the tens of million of dollars. The others are smaller, some offering only one product. All of them are private companies so measuring their actual sales numbers is a bit difficult. It may well be that a couple of companies on the list do in fact sell more than ten million worth of products in a fiscal year. if so my apologies to the VP of Marketing that will be getting in touch with me.

Atrenta (www.atrenta.com) has diversified its products line and openly identifies only one of its products, as using assertion based technology. In fact formal tools are used in all of its products, including SpyGlass the earliest and most well known of them. Atrenta is large enough that rumors have circulated in the industry for some time about the company wish to go public. Unfortunately the size of the market served and the very high level of competition in EDA make the timing of such a move very delicate and almost certainly would not generate the desired level of returns for its founders and early investors.

Jasper Design Automation (www.jasper-da.com) also offers more than one product and proudly identifies them as formal tools. The company has found good acceptance in the market and has been talked about as a possible acquisition target. So far it has not fallen to the promises of its suitors and may in fact find ways to reward those involved with the company in different ways.

Either company may be a target of acquisition not for their technology but for their presence in the market. At this time the big three EDA market leaders can successfully co-exist with these two in their corporate accounts. But any financial "disturbance" in those accounts would trigger a determined acquisition effort.

OneSpin Solutions (www.onespin-solutions.com) is a European company and suffers from the same drawbacks as practically all such companies. It must continue to improve its presence in the American market, something that is costly and depends highly on the capabilities of those hired to achieve this result. Unfortunately, as it has been proven multiple times, technology does not sell itself. Technological superiority is required but not sufficient to establish a product in the market. During my long career I saw many less advanced products become popular and financially successful at the expense of tools with better technology.

Averant (www.averant.com), Avery Design Systems (www.avery-design.com), and Axiom Design Automation (www.athdl.com) offer multiple formal verification and validation tools, while Assertive

Design (www.assertivedesign.com), Jeda Technologies (www.jedatechnologies.net), and Zocalo Tech (www.zocalo-tech.com) have one formal product each.

Although Real Intent and Blue Pearl Software also can be classified in the formal validation market they are different. Blue Pearl Software (www.bluepearlsoftware.com) offers products for the FPGA users. In addition to verification products it also has a timing constraints product. Real Intent (www.realintent.com) started as a solely formal verification company. It has found a way to morph itself and uses formal techniques to provide power analysis and clock domain analysis. It has found the shift in its marketing strategy profitable.

SLEC was Calypto's (www.calypto.com) first product. It is an equivalence checking tool that has been significantly strengthened through the years. The company has inherited the Catapult product from Mentor. In addition it also has a power analysis and optimization product. It is clearly diversifying and establishing a presence in the ESL market as well.